IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Liu, *et al.*	Docket No.:	TSM03-0454
Serial No.:	10/823,159	Art Unit:	2814
Filed:	April 13, 2004	Examiner:	Marcos D. Pizarro Crespo
For:	Via Recess In Underlying Conductive Line		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF INVENTOR UNDER 37 C.F.R. § 1.132

Dear Sir:

I, Chung-Shi Liu, am an inventor for the inventions of Claims 1-27 of the present application, U.S. Application Serial No. 10/823,159.

The depth of the via recess is critical to the reliability and yield of the semiconductor device formed using the inventions of Claims 1-27 of the present application. A critical depth range for the via recess is between about 100 angstroms and about 600 angstroms, to improve performance, reliability, and yield. A more optimized and preferred depth range for the via recess, within the critical depth range, is between about 150 angstroms and about 300 angstroms.

Too much via recess will damage the conductive line. If the conductive line is formed from copper, for example, as is now common practice, a via recess formed too deeply is more likely to induce copper stress migration failure. On the other hand, having the via recess too shallow is more likely to induce current crowding and electron migration failure. Thus, the depth of the via recess is critical.

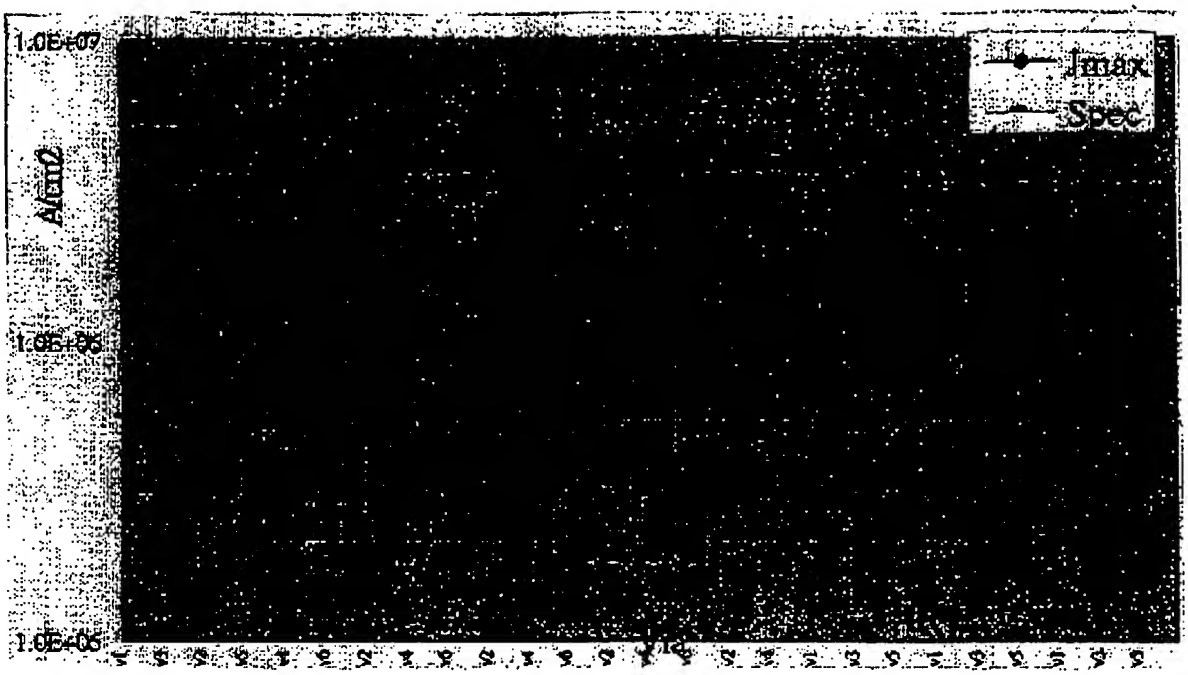
The following is evidence of this optimized and preferred depth range. Tests were performed with a recess of 90Å, 250Å, 700Å, and 900Å. Stress migration failure tests were performed in structures having these three recess depths: 90Å, 250Å, and 700Å. The table below shows the results of the stress migration failure tests:

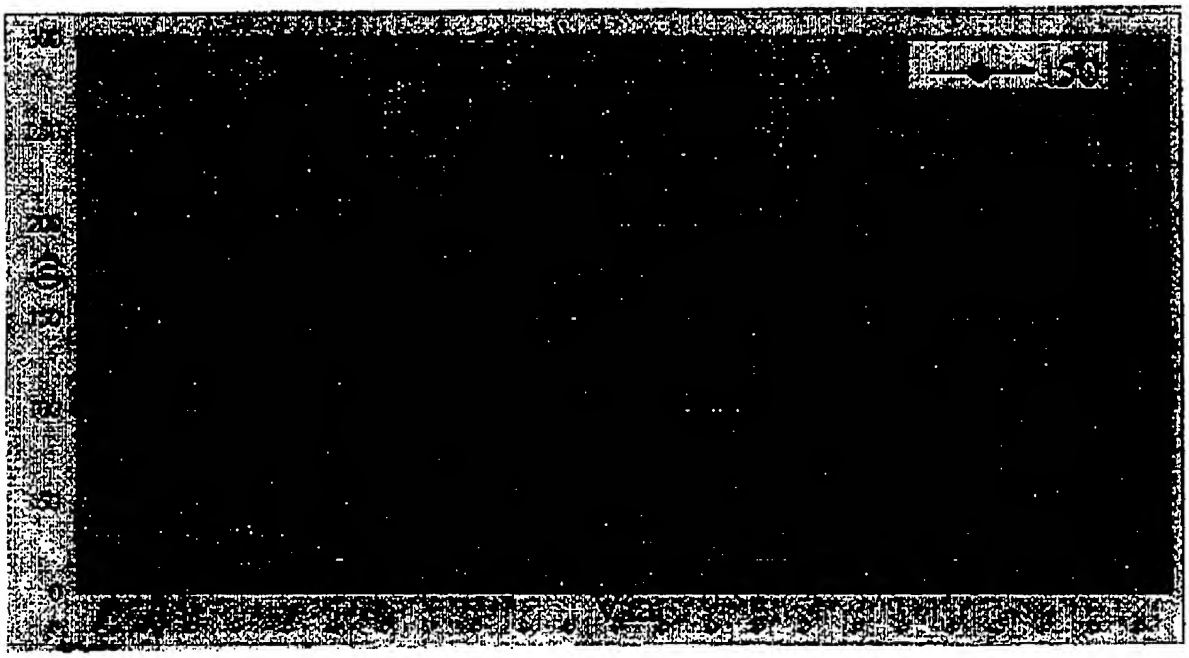
	Rs shift	1	2	3	4
Cu recess depth (Å)		700	700	250	90
Stress Migration Fail Die	>10% (Ref.)	15	16	1	0
	>500% (fail)	14	16	1	0
Number of dies tested		96	96	96	96

The data shown in the chart above shows the number of failed die out of 96 tested for each recess depth (for each column).

Based on the data shown in the table above for stress migration failure tests, the structures with a 700Å recess depth exhibited poor results compared to the same structures having 90Å and 250Å recess depths. Thus, structures having a recess depth less than 700Å perform better under stress migration tests.

Electron migration failure were performed in structures having these three recess depths: 90Å, 250Å, and 900Å. The two charts below show the results of these electron migration failure tests. In the first chart, J_{max} is the maximum electron migration current allowed in the circuit. A larger J_{max} value is better. In the second chart, t_{50} is the mean time to failure on the testing condition. A longer mean time t_{50} is better.





Based on the data shown in the charts above for electron migration failure tests, the structures with a 90Å recess depth exhibited poor results compared to the same structures having 250Å and 900Å recess depths. Thus, structures having a recess depth greater than 90Å perform better under electron migration tests.

Hence when considering both stress migration and electron migration performance, the best range of depth for the recess depth is greater than 90Å and less than 700Å.

Forming a via recess in accordance with Claims 1-27 within the critical depth range produces unexpected increases in device performance, reliability, and production yield, which to the best of my knowledge is new. The prior art known to me, and the prior art cited in the office action, do not disclose this critical depth range, that this depth range is critical, and the unexpected results of using this new critical depth range.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

July 20, 2006
Date signed

Chung-Shi Liu
Chung-Shi Liu, Inventor